AN-720
Application Note

INTERFACING WITH MECL 10,000 INTEGRATED CIRCUITS

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This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as; input impedance, output drive, gain, and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling of non-compatible signals.

MOTOROLA Semiconductor Products Inc.

INTERFACING WITH MECL 10,000 INTEGRATED CIRCUITS

INTRODUCTION

The MECL 10,000 series is a high speed logic family designed for applications where system performance is important. Emitter coupled logic is used to obtain the required circuit speed and provide the circuit features necessary to optimize high speed system design. All MECL 10,000 circuits interface directly with each other. In addition, MECL 10,000 circuits are completely compatible with the very fast MECL III circuits, permitting a designer to mix both families in the same system for best performance.

MECL 10,000 circuits normally operate with ground on V_{CC} and a negative 5.2 Vdc power supply on V_{EE}. While MECL may be used with ground on V_{EE} and +5 Vdc on V_{CC}, the negative supply operation has noise immunity advantages and is recommended for larger systems. Also, emitter coupled logic operates with a relatively small 800 mV logic swing. With the -5.2 volt power supply the normal MECL 10,000 high logic level is about -0.9 volt and the low logic level about -1.7 volts. For these reasons MECL 10,000 and MECL III are not directly compatible with the common slower speed logic types such as TTL, DTL, and MOS. Translators must be used when interfacing these logic types with MECL.

In many designs it is necessary to interface with signals which are not digital logical levels. These may be low amplitude input signals which must be amplified before they can be used and low frequency signals which require shaping. The linear characteristics of the MECL line receivers allow these circuits to be used as amplifiers or Schmitt triggers.

Another important interface requirement is driving optic displays. The MECL 10,000 outputs are directly compatible with light emitting diode requirements. MECL circuits are also available for driving other types of displays.

INTERFACING WITH TTL

The most common interface requirement for MECL is with TTL logic levels. This occurs when a MECL system must interface with an existing TTL system or when both MECL and TTL are used in the same system design. The interface requirements between MECL and TTL depend on how the circuits are being used.

The normal MECL/TTL interface occurs when MECL is powered with a -5.2 volt power supply and TTL with +5 volts. The use of a common ground and separate power supplies helps isolate TTL generated noise from the MECL supply lines. The MECL/TTL translator circuits, MC10124 and MC10125, shown in Figure 1 provide this interface.

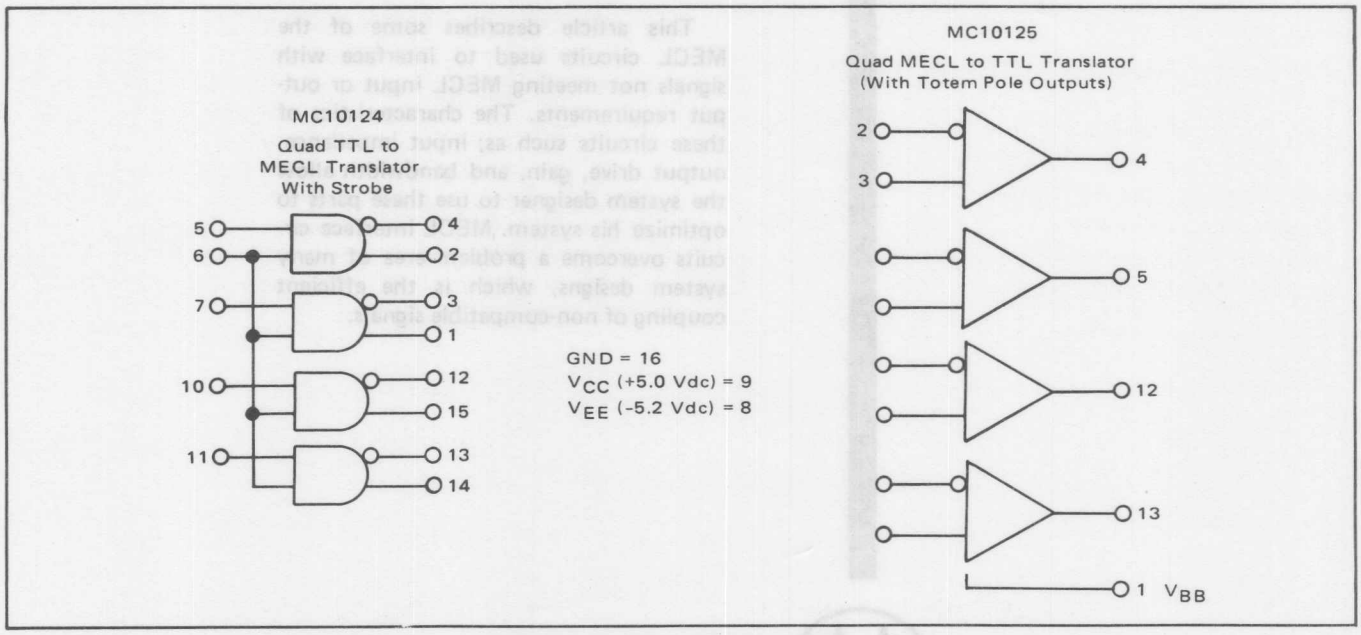

FIGURE 1 – MECL/TTL Translators

The MC10124 is a quad TTL to MECL translator, with a common TTL strobe input and complementary MECL outputs. The propagation delay through the circuit is typically 5 ns and the top operating frequency is normally greater than 85 MHz. If maximum operating frequency tests are made with the 5.5 ns input rise and fall times specified on the component data sheets, operating speed is limited to 70 MHz because of input restrictions. With faster rise and fall times on the inputs, circuit speed increases until the output fails to reach specified limits at about 85 MHz.

The MC10125 is a quad MECL to TTL translator with differential amplifier inputs and Schottky clamped transistor "totem pole" TTL outputs. Propagation delay time for the circuit is a function of fan-out loading as shown by the curves in Figure 2. As with the MC10124, maximum operating frequency is limited by the output failing to reach specified output levels above 85 MHz.

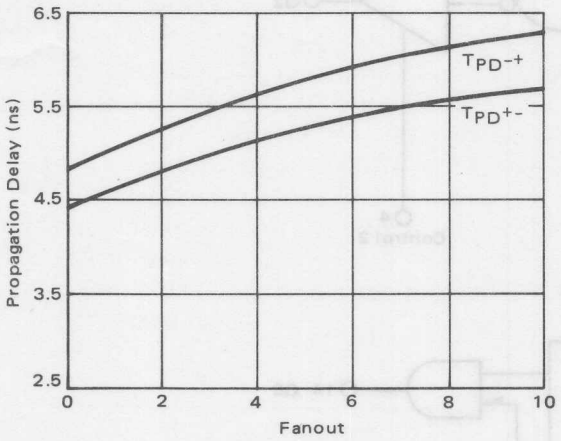

FIGURE 2 – Propagation versus Fanout for the MC10125

A feature of the MC10124/MC10125 pair is the ability to operate over long distances with a twisted pair line. Figure 3 shows the flexibility of using these parts with twisted pair lines as any combination of MECL and TTL inputs and outputs can be interfaced with MECL signal levels on the interconnecting lines.

The complementary outputs of a MECL gate or the MC10124 translator and the differential inputs of a MECL line receiver or the MC10125 translator are used with a twisted pair line to send signals over long distances. Since the line receiver looks at the voltage difference between the two input signals and not the absolute value, the circuit has good noise rejection capability. A noise pulse coupling into the twisted pair line appears equally on both of the line receiver inputs and is rejected as common mode noise. The differential operation is also advantageous when two sections of a system are not connected with a solid ground or power line. The power supply offset appears as common mode signal to the receiver and is rejected within the limits of the receiver. The MECL to TTL translator typically rejects common mode signals greater than plus or minus 2.5 volts before the output fails to remain within specified limits.

When high speed signals are transmitted on long lines, termination techniques should be used to minimize reflections and waveform distortion. These reflections cause ringing on the signal line which if severe enough will effect system noise immunity. The designer should consider using termination resistors when the two way propagation time of the line is greater than the rise time of the signal on the line for best system performance. Figure 3 shows the use of a parallel termination resistor, R_T, at the receiving end of the line. The value of R_T should match the line impedance which is about 110 ohms for common twisted pair lines.

A common application for the MECL translators is high speed line drivers and receivers in an all TTL system. The TTL system sees only the translator TTL inputs and outputs, but takes advantage of MECL line driving capabilities to send signals from one point to another in the system. The gain of the MC10125 is typically greater than 15 volts per volt making the circuit a useful input device for interfacing to TTL logic levels.

INTERFACING WITH TTL BUSSES

In many system designs it is necessary to tie several pieces of equipment together with input/output bus lines. These lines are time shared with the various sections of

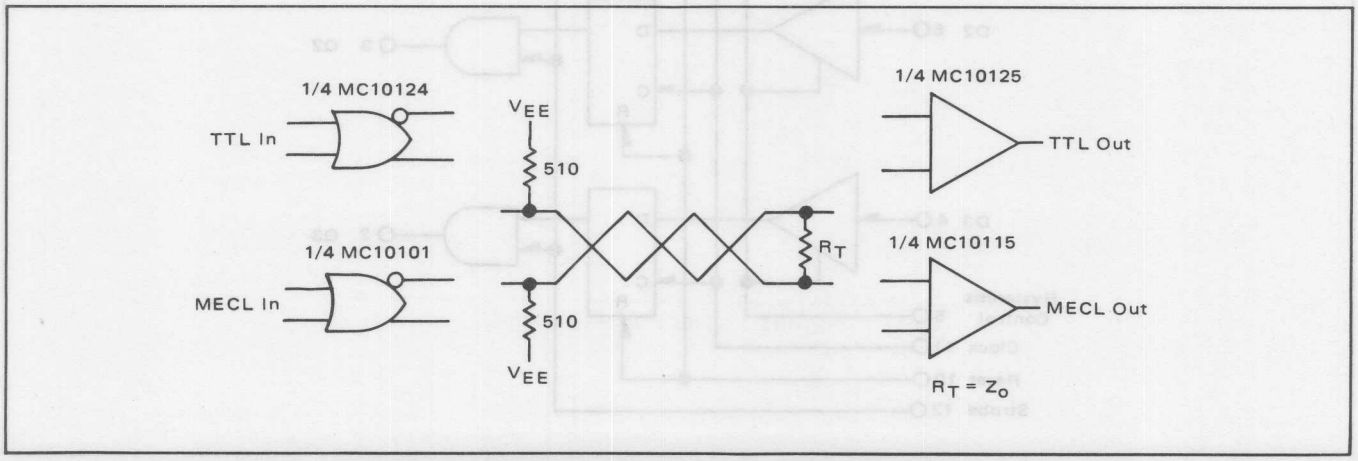

FIGURE 3 – Use of Twisted Pair Line with MECL and TTL Signals

the total system, requiring that only one line driver be active at a time. Three state TTL is commonly used in these applications because of the ability to disconnect the driver from the line. When disabled, the driver does not appear as a heavy load to the active driver or as a low impedance discontinuity to the bus line. The MC10128 Bus Driver and MC10129 Bus Receiver shown in Figure 4 are designed to interface a high speed MECL system into a TTL compatible bus line.

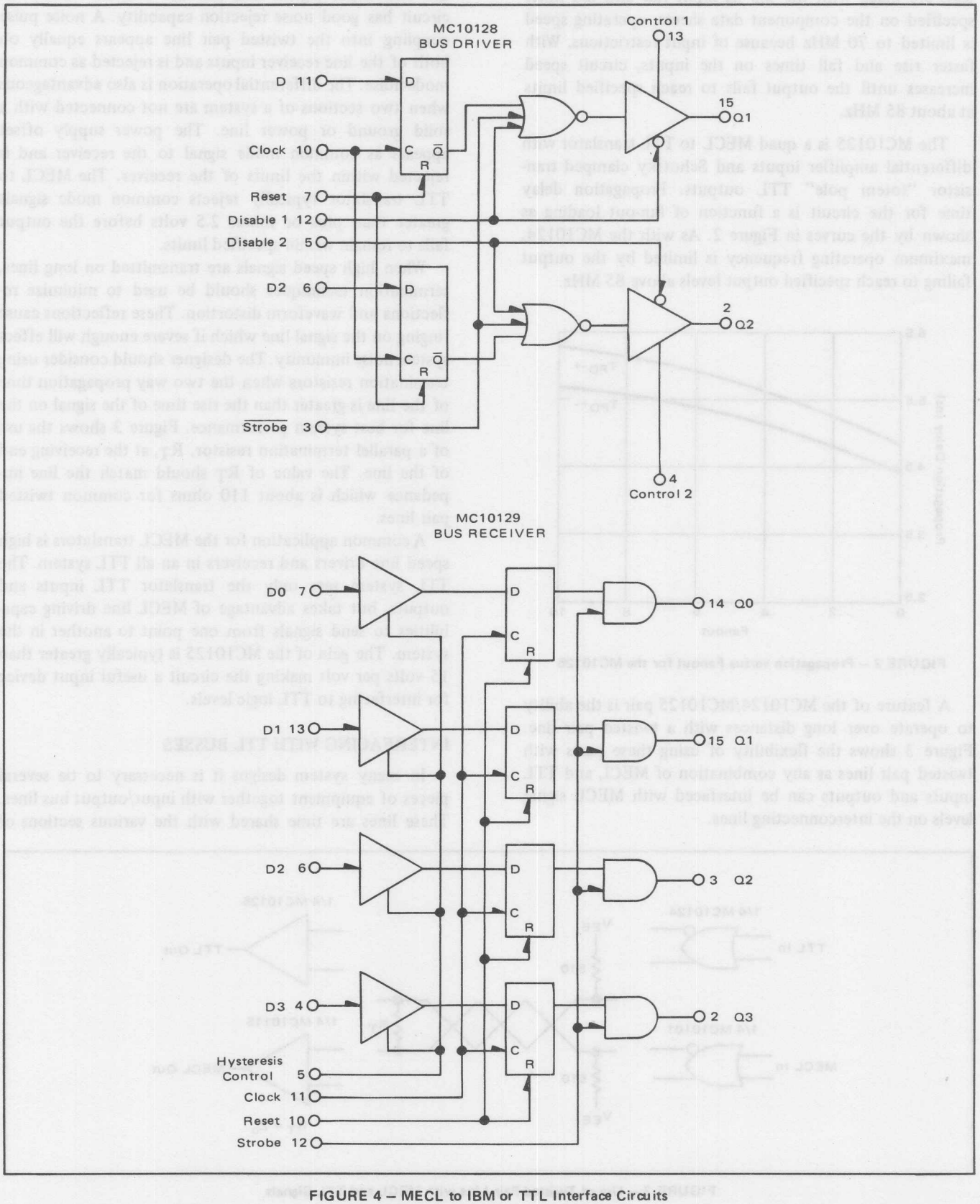

FIGURE 4 – MECL to IBM or TTL Interface Circuits

The MC10128 is a dual bus driver with MECL inputs. Internal latches are provided to free the data inputs while waiting for the information to be used. When the clock input is held at a low logic level or left unconnected data passes through the latch. Disabled inputs are provided for each bus driver to control the three state output. A high MECL logic level on a disable line causes the driver output to go to a high impedance state overriding the strobe, but the clock and data inputs can still be used with the latch.

Leakage current into a disabled output is important when interfacing with TTL three state drivers since the TTL circuits are commonly rated at 2 mA and 2.4 volts for a high level output. The curve in Figure 5 shows typical leakage current of the MC10128 bus driver with the output disabled. This current should be considered when figuring loading on a TTL driver. The MECL part is rated for 50 mA at 2.5 volts, therefore loading is not a problem for the MC10128 driving disabled outputs.

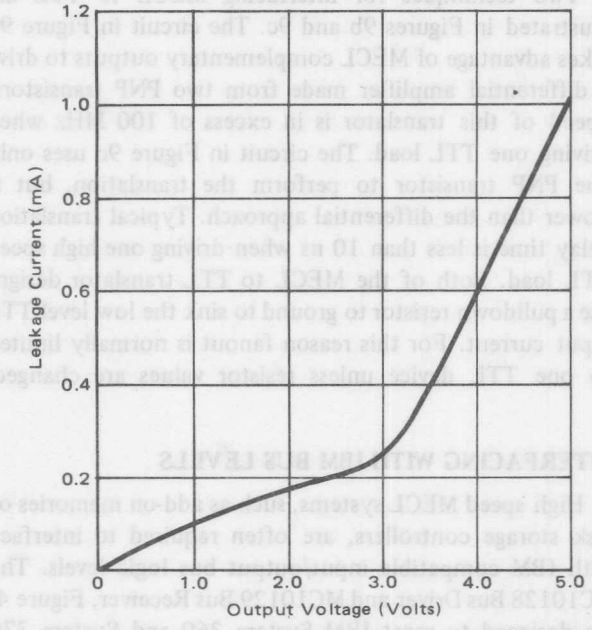

FIGURE 5 – Output Current into a Disabled MC10128 Bus Driver

The MC10128 bus drivers have control inputs which control the mode of circuit operation. When a control input is left open the bus driver operates in a TTL compatible bus system. With a grounded control input the bus driver outputs are compatible with IBM System 360 I/O bus requirements. IBM compatibility will be discussed in a following section.

The MC10129 quad bus receiver accepts TTL or IBM bus logic levels and translates to MECL outputs. Internal latches are provided to free the bus lines while waiting for the data to be used. The circuit features a hysteresis control input which changes the threshold points for circuit switching as shown in Figure 6. In normal operation the hysteresis input is connected to V_{EE} giving guaranteed input threshold points of 2.0 volts for a high logic level, and 0.8 volt for a low level with TTL inputs (1.7 volts and 0.7 volt with IBM bus inputs). Figure 6a shows the transfer characteristics when the hysteresis feature is not used.

In a high noise environment hysteresis is added to the circuit by connecting the hysteresis control input to ground. In the hysteresis mode high level threshold points are specified at 2.6 and 1.9 volts. The circuit is guaranteed to recognize a high level input below 2.6 volts, but the input may drop to 1.9 volts and remain a guaranteed high level. The low level threshold points are 1.0 volts and 1.7 volts. Typical transfer characteristics and specified MC10129 threshold points in the hysteresis mode are shown in Figure 6b. The hysteresis is the input difference between the rising and falling output edges and is nearly 700 mV in the figure.

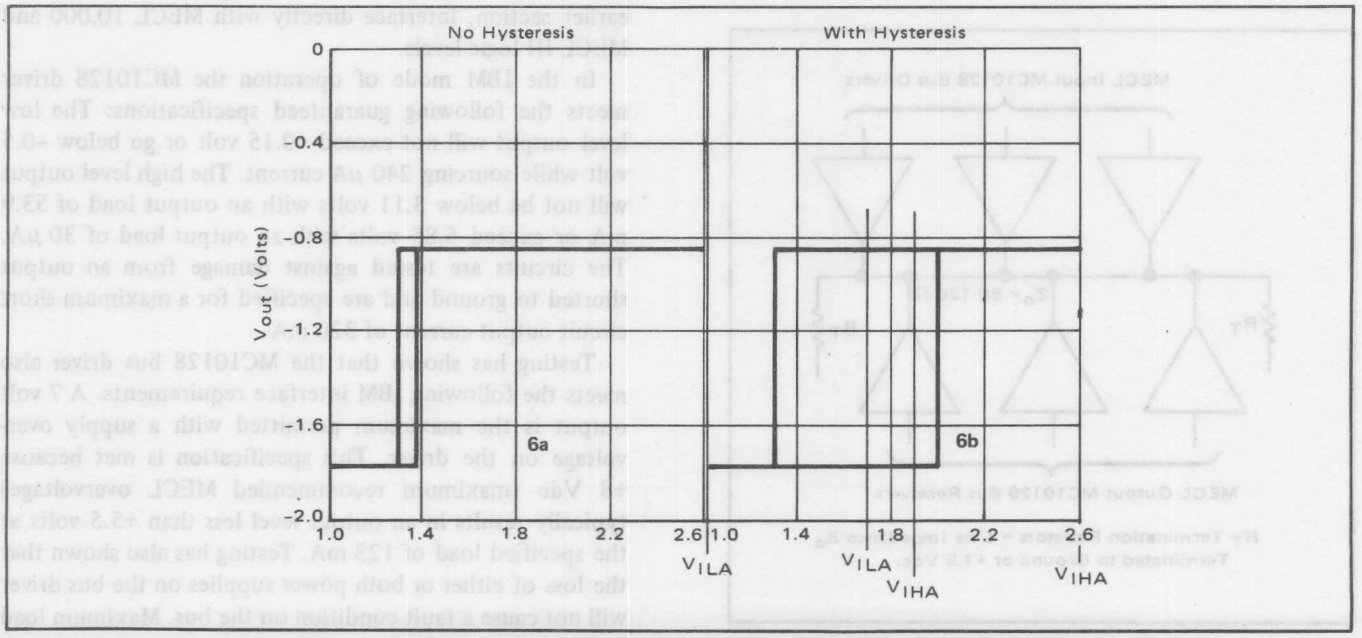

FIGURE 6 – Transfer Characteristics of the MC10129 Bus Receiver

Figure 7 illustrates a bus line using both TTL and MECL bus driver and receiver citcuits. Any standard pull up or termination resistor network presently used on the TTL bus will be compatible with the MC10128. Thus with the MC10128 and MC10129 it is possible to directly interface a high performance MECL system into many existing minicomputer I/O bus lines.

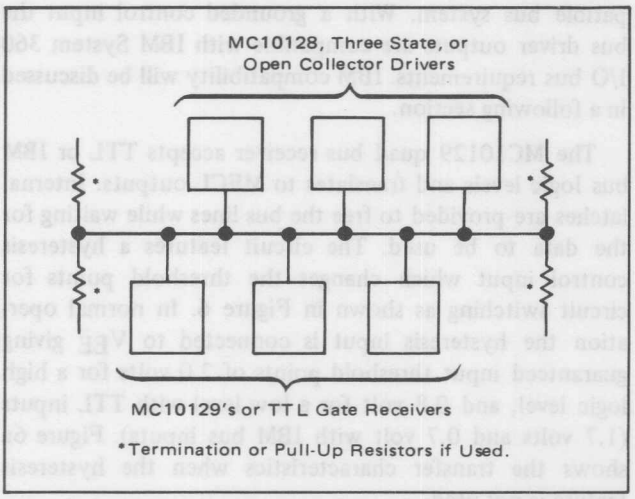

FIGURE 7 – MECL/TTL Bus Line

The MECL bus driver and receiver circuits can also be used to build bus lines in an all MECL system as shown in Figure 8. The MC10128 bus driver is specified driving 50 ohms to ground or 25 ohms to +1.5 Vdc. A 100 ohm bus would be terminated by a 100 ohm resistor to ground at each end, or a 50 Ω bus by 50 ohm resistors to +1.5 Vdc at each end. An alternate to the +1.5 V supply is a resistor equivalent of 68 Ω to ground and 160 Ω to +5 Vdc. The terminated bus allows high speed data transfer because it is not necessary to allow time for reflections on the line to settle out. Normally a TTL output is not able to drive a bus terminated as shown in Figure 8.

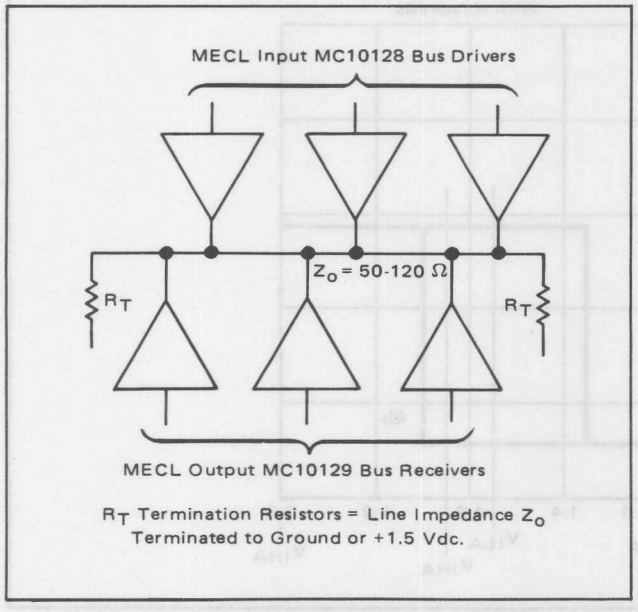

FIGURE 8 – MECL System Bus Line

INTERFACING WITH TTL ON A COMMON POWER SUPPLY

In many system designs where a small number of MECL circuits are used, it is desirable to operate both MECL and TTL on a +5 Vdc power supply. MECL works very well in this mode if care is taken to isolate the TTL generated noise from the MECL +5 volt supply line. Translators for interfacing TTL and MECL in this mode are built with discrete components since integrated circuit translators do not operate on a single +5 volt supply.

The TTL to MECL translator shown in Figure 9a consists of three resistors in series to attenuate TTL outputs to MECL input requirements. The translation is very fast, normally under 1 ns, depending on wiring delays and stray capacitance.

Two techniques for interfacing MECL to TTL are illustrated in Figures 9b and 9c. The circuit in Figure 9b takes advantage of MECL complementary outputs to drive a differential amplifier made from two PNP transistors. Speed of this translator is in excess of 100 MHz when driving one TTL load. The circuit in Figure 9c uses only one PNP transistor to perform the translation, but is slower than the differential approach. Typical translation delay time is less than 10 ns when driving one high speed TTL load. Both of the MECL to TTL translator designs use a pulldown resistor to ground to sink the low level TTL input current. For this reason fanout is normally limited to one TTL device unless resistor values are changed.

INTERFACING WITH IBM BUS LEVELS

High speed MECL systems, such as add-on memories or disk storage controllers, are often required to interface with IBM compatible input/output bus logic levels. The MC10128 Bus Driver and MC10129 Bus Receiver, Figure 4, are designed to meet IBM System 360 and System 370 I/O interface requirements. These circuits, described in an earlier section, interface directly with MECL 10,000 and MECL III logic levels.

In the IBM mode of operation the MC10128 driver meets the following guaranteed specifications: The low level output will not exceed +0.15 volt or go below -0.5 volt while sourcing 240 μA current. The high level output will not be below 3.11 volts with an output load of 53.9 mA or exceed 5.85 volts with an output load of 30 μA. The circuits are tested against damage from an output shorted to ground and are specified for a maximum short circuit output current of 320 mA.

Testing has shown that the MC10128 bus driver also meets the following IBM interface requirements. A 7 volt output is the maximum permitted with a supply over-voltage on the driver. This specification is met because +8 Vdc (maximum recommended MECL overvoltage) typically results in an output level less than +5.5 volts at the specified load of 123 mA. Testing has also shown that the loss of either or both power supplies on the bus driver will not cause a fault condition on the bus. Maximum load current occurs with a positive supply shorted to ground

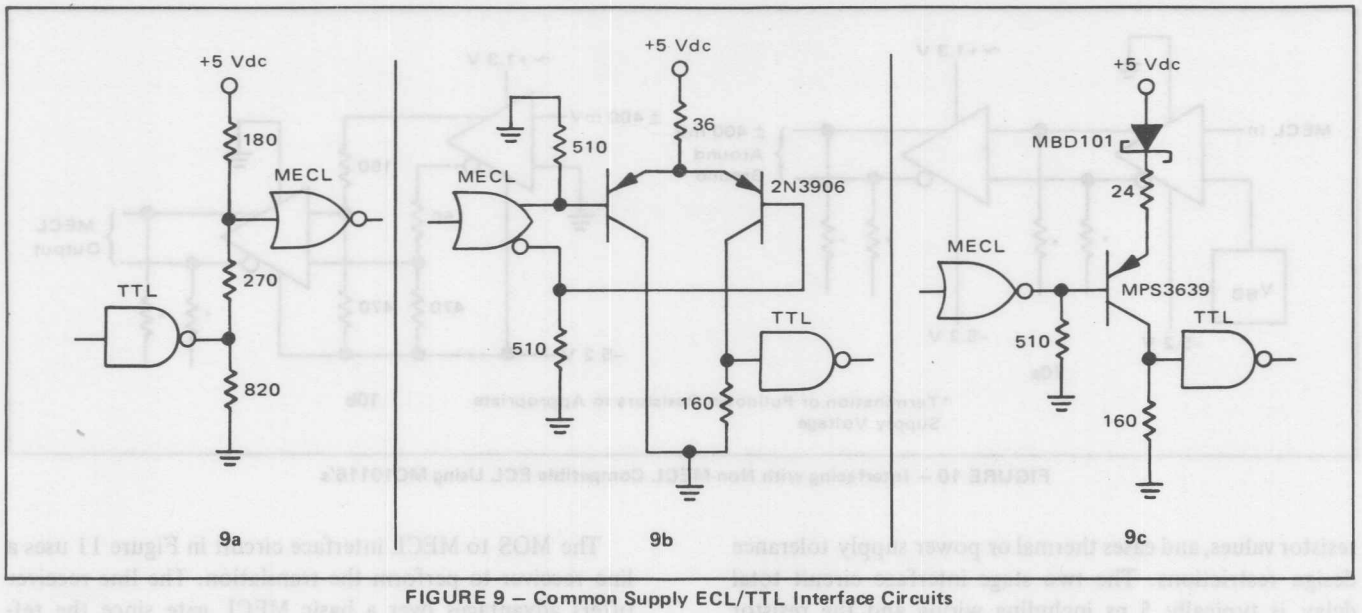

FIGURE 9 – Common Supply ECL/TTL Interface Circuits

and this is typically less than 4 mA with +6 volts on the bus line or less than 1 mA with 5 volts or less on the bus.

The MC10129 bus receiver is designed to translate IBM compatible bus lines to MECL logic levels. The high and low input logic level threshold points are specified at +1.7 volts and +0.7 volt to give IBM specified noise margins. The input current requirements for the MC10129 are well below IBM maximum specifications. At a high input level of 3.11 volts the MC10129 input current is less than 95 μA and the low level input current at 0.15 volt is not below -1.0 μA. This compares with 420 μA and -240 μA for the IBM specifications.

Testing has shown compatibility with most other IBM specification requirements. The circuit will withstand 7 volts on the bus input with power applied, although input current may be as high as 30 mA with a 7 volt input. The MC10129 has no problem meeting the -0.15 volt on the input either power up or power down. IBM's requirement of 6 volts on the receiver input with no power on the MC10129 is not met if the V_{CC} line on the receiver is shorted to ground. With the positive supply open, the 6 volt requirement is met, but input current can exceed 25 mA. This specification may be met by using a series resistor of 510 to 1000 ohms between the bus line and the receiver input. This limits current into the line receiver during a power down condition. Another IBM specification not directly met is the input impedance requirement of greater than 4 k ohms and less than 20 k ohms. Typical input impedance of the MC10129 is approximately 50 k ohms with a high level of 3.11 volts on the bus. If this interface requirement is necessary, a 20 k ohm resistor between the MC10129 input and ground provides an input impedance within specified limits.

The MC10128 and MC10129 bus drivers and receivers give the MECL system designer the capability to interface with the input/output requirements of many system types. In addition these parts can be used for bus lines interconnecting sections of large MECL systems.

INTERFACING WITH ECL OPERATING AT NON-MECL POWER SUPPLY VOLTAGES

MECL circuits are sometimes required to interface with ECL systems operating at power supply voltages that differ from the standard MECL ground and -5.2 volts. These circuits commonly use ground for a bias reference voltage, resulting in a logic swing centered around ground. This signal can be converted to and from MECL 10,000 logic levels with MECL line receivers and proper use of available power supplies.

MECL signals can be shifted more positive as shown in Figure 10a. The first line receiver stage generates complimentary signals and is unnecessary when MECL complimentary signals are available at the input. The second line receiver is powered by the MECL -5.2 volts on V_{EE} and the +1.3 volts on V_{CC} from other ECL circuits. The complimentary outputs from the first stage present a differential signal to the second stage within the common mode range of the circuit. The line receiver doing the translating operates at a total supply voltage of 6.5 volts, which is no problem for a low power line receiver circuit such as the MC10116.

The circuit in Figure 10b may be used to translate down to MECL input requirements. A line receiver connected to +1.3 volts and -5.2 volts is used to generate complementary outputs and amplify the signal prior to using a voltage divider to the second stage. Due to the differential operation of the MC10116 line receiver, the +1.3 volt supply is not critical and any value between +1.0 and +1.5 volts is acceptable. With the power on the circuit elevated to 6.5 volts, typical output swing is greater than 900 mV. The resistor divider network shifts the signals to MECL levels as required by the second line receiver stage. This stage, operating at normal MECL power supply levels, delivers normal MECL output signals. The use of differential signals is recommended in the voltage dropping network as this eliminates the need for critical

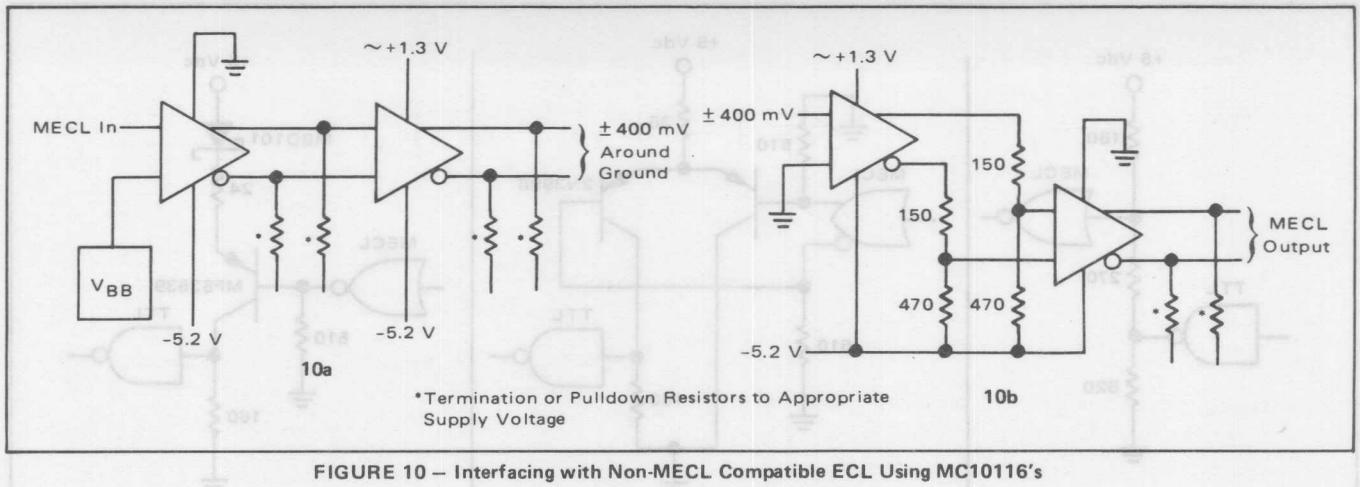

FIGURE 10 – Interfacing with Non-MECL Compatible ECL Using MC10116's

resistor values, and eases thermal or power supply tolerance design restrictions. The two stage interface circuit total delay is typically 5 ns including wiring and the resistor dividers. (The MC10116 has a typical propagation delay of 2 ns per stage.)

Another circuit that can be used to translate a signal swing around ground to MECL logic levels is the MC1650. This MECL III part is a high speed dual A/D comparator which is ideal for this interface, but designers should consider the cost and capability of the MC1650 against system requirements to determine the best interface circuit.

MECL/MOS INTERFACE CIRCUITS

The MECL/MOS interface varies with the type of MOS and the MOS power supply voltages. For P-channel MOS circuits operating between ground and a negative voltage, the circuits shown in Figure 11 may be used. The diode in the MECL to PMOS translator biases the PNP transistor off and on with MECL logic levels, as the transistor amplifies the MECL logic swing to the large P-channel MOS requirements.

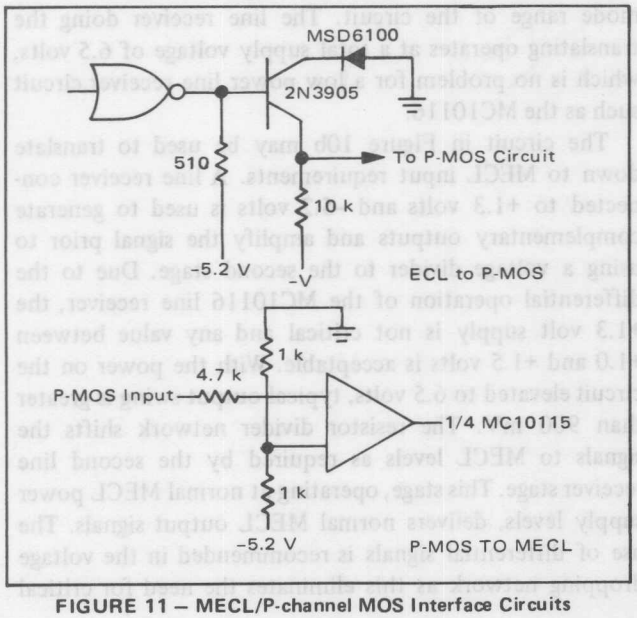

FIGURE 11 – MECL/P-channel MOS Interface Circuits

The MOS to MECL interface circuit in Figure 11 uses a line receiver to perform the translation. The line receiver offers advantages over a basic MECL gate since the reference voltage can be made more negative with the resistor divider, and the receiver input is a lighter load for a P-MOS output due to the absence of internal pulldown resistors. The 4.7 k resistor is used to limit input current when the MECL input clamps at about -6 volts in the negative direction.

Modern N-channel circuits are commonly TTL compatible, and CMOS at +5 volts operates with TTL logic levels. The MECL/TTL translators (MC10124 and MC10125) or the MECL bus circuits (MC10128 and MC10129) described earlier perform these interface requirements. The MC10129 bus receiver is especially useful as a MOS to MECL translator because the low input current requirements of the MC10129 (typically 60 μA at 3 volts) does not load the MOS circuits as would a normal TTL circuit input.

MOS Memory systems often require using many MOS packages to obtain required memory capacity. These memory circuits have a common clock line that requires a large voltage swing (10 to 20 volts), and the combined capacitance of many MOS inputs. The MC10127 dual MECL to MOS translator is designed to meet this system interface requirement. This circuit takes MECL levels on the input and drives MOS circuits with a supply voltage up to 20 Vdc, and typically has a 20 ns propagation delay when driving a 350 pF load.

This availability of interface circuits allows the designer to take advantage of both MECL performance, and the low power and high circuit density of MOS for the slower sections of a system.

LOW LEVEL SIGNALS TO MECL

The differential amplifier operation of MECL line receivers permits these circuits to amplify low level signals to MECL logic levels. The circuit in Figure 12 is a typical amplifier design which uses the MC10116 line receiver to receive signals as low as 50 mV and give good MECL outputs. This design features two 100 ohm resistors in parallel for a 50 ohm input impedance to AC signals. The

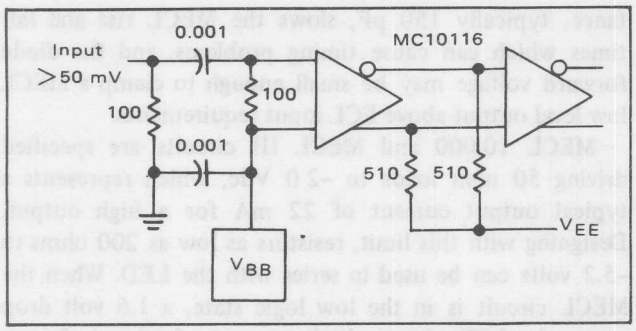

FIGURE 12 – Low Level Amplifier Using a MECL Line Receiver

resistor values can be adjusted to terminate other wire impedances. Capacitor coupling is recommended for operation with signals that do not swing around a center point equal to the V_{BB} reference voltage.

The maximum bandwidth of the amplifier depends on the MECL line receiver part type as shown in the circuit gain versus operating frequency curves in Figure 13. The lowest frequency part that meets system requirements should be selected to lower component cost and ease design rules. For example, the MC1692 should be limited to two cascaded stages and short interconnection lines to insure circuit stability. Also, the MC1692 is more stable in the stud "S" package than the dual in-line "L" package when used as an amplifier. Cascading three or more stages is possible with the slower MC10116 or MC10115 line receiver circuits.

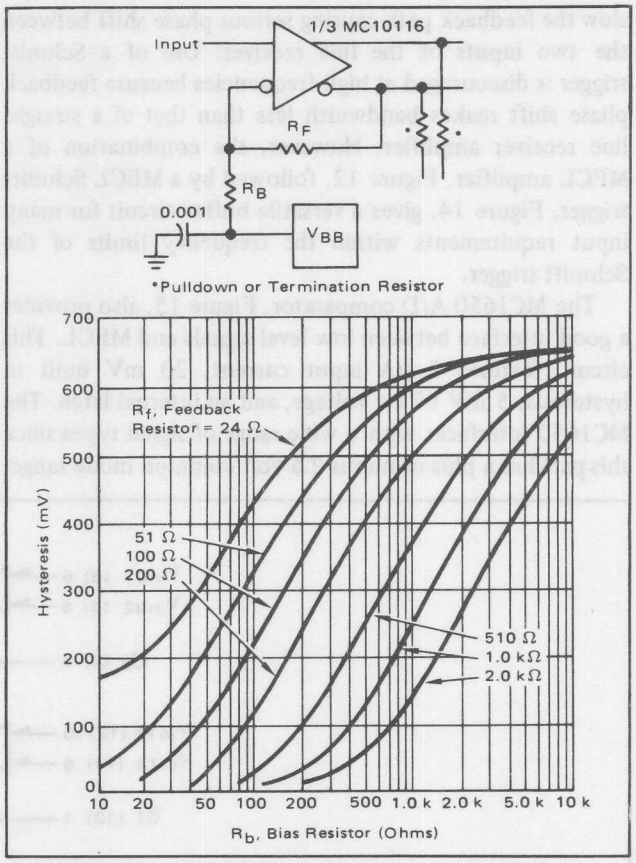

FIGURE 14 – MECL Schmitt Trigger and Hysteresis Curves

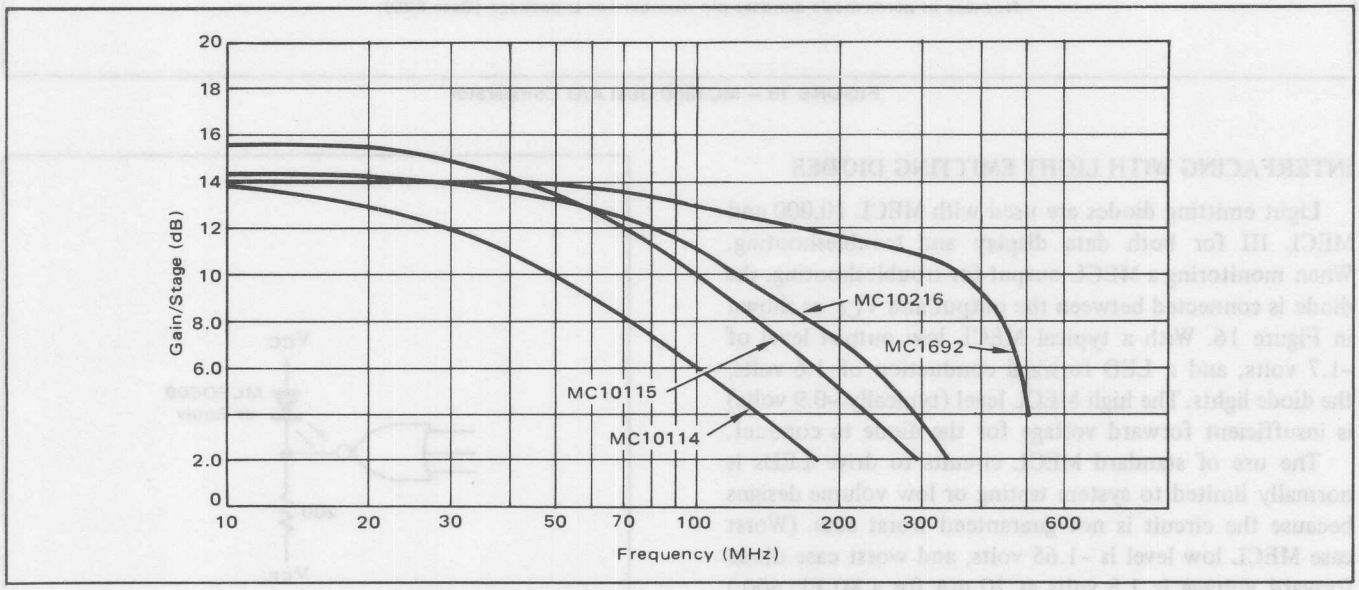

FIGURE 13 – Gain versus Frequency for MECL Line Receivers

MECL line receiver circuits can also be connected as Schmitt triggers to shape low frequency signals to MECL rise and fall times. An MC10116 connected as a Schmitt trigger is illustrated in Figure 14. The table in the figure shows the amount of hysteresis as a function of the feedback resistors. For low frequency signals below 1 kHz at least 150 mV of hysteresis should be used to insure the circuit does not momentarily oscillate during the output transition.

When connecting a line receiver as a Schmitt trigger it is important that the feedback resistors be connected to an inverting output from the input signal. If this is not followed, the performance of the input signal will be degraded because of negative, instead of positive, feedback. When the Schmitt trigger must also handle higher frequencies it is necessary to restrict the values of the feedback resistors. Above 50 MHz the resistors should be limited to 200 ohms or less, so stray capacitance does not

slow the feedback path causing serious phase shift between the two inputs of the line receiver. Use of a Schmitt trigger is discouraged at high frequencies because feedback phase shift makes bandwidth less than that of a straight line receiver amplifier. However, the combination of a MECL amplifier, Figure 12, followed by a MECL Schmitt trigger, Figure 14, gives a versatile buffer circuit for many input requirements within the frequency limits of the Schmitt trigger.

The MC1650 A/D comparator, Figure 15, also provides a good interface between low level signals and MECL. This circuit features 3 μA input current, 20 mV built in hysteresis, 5 mV offset voltage, and an internal latch. The MC1650 interfaces with a wide range of signal types since this part has a plus or minus 2.5 volt common mode range.

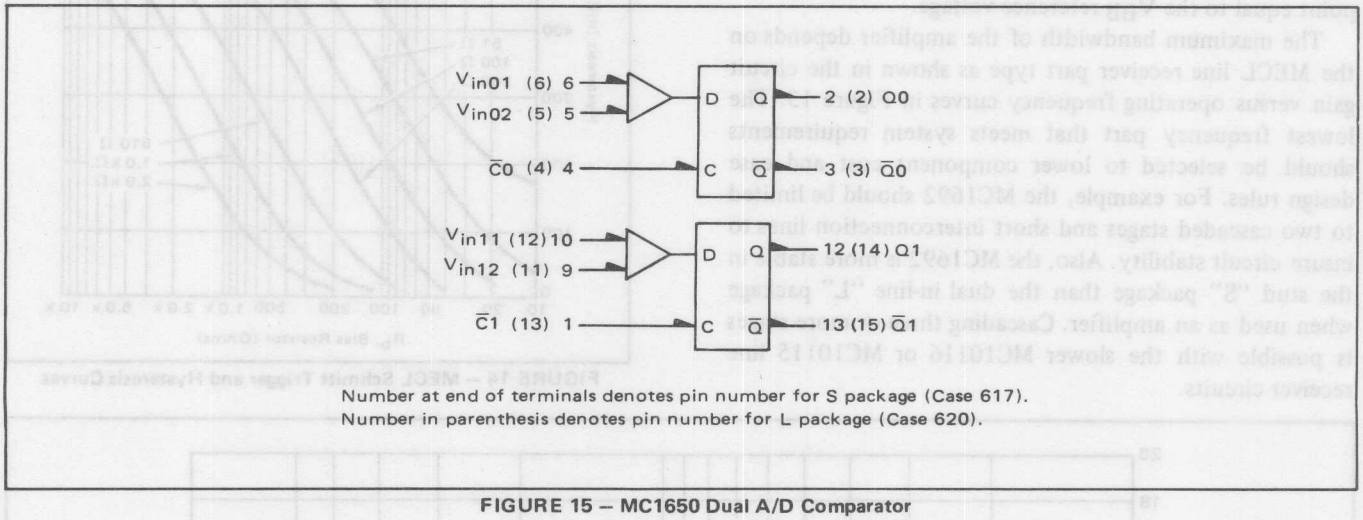

FIGURE 15 – MC1650 Dual A/D Comparator

INTERFACING WITH LIGHT EMITTING DIODES

Light emitting diodes are used with MECL 10,000 and MECL III for both data display and troubleshooting. When monitoring a MECL output for troubleshooting, the diode is connected between the output and V_{CC} as shown in Figure 16. With a typical MECL low output level of -1.7 volts, and a LED forward conduction of 1.6 volts, the diode lights. The high MECL level (typically -0.9 volts) is insufficient forward voltage for the diode to conduct.

The use of standard MECL circuits to drive LEDs is normally limited to system testing or low volume designs because the circuit is not guaranteed worst case. (Worst case MECL low level is -1.65 volts, and worst case diode forward voltage is 1.8 volts at 20 mA for a MLED 600.)

When LEDs are driven from MECL for data display, the MC10123 bus driver should be used. This circuit has a guaranteed low logic level output of -2.03 to -2.10 volts and a worst case high level of -0.960 volt. These levels are compatible with standard LED worst case requirements.

Generally, it is not advisable to drive another MECL circuit from an output driving a LED. The diode capacitance, typically 150 pF, slows the MECL rise and fall times which can cause timing problems, and the diode forward voltage may be small enough to clamp a MECL low level output above ECL input requirements.

MECL 10,000 and MECL III circuits are specified driving 50 ohm loads to -2.0 Vdc, which represents a typical output current of 22 mA for a high output. Designing with this limit, resistors as low as 200 ohms to -5.2 volts can be used in series with the LED. When the MECL circuit is in the low logic state, a 1.6 volt drop across the LED gives a diode current of 18 mA. Larger resistor values are used when less diode current is desired.

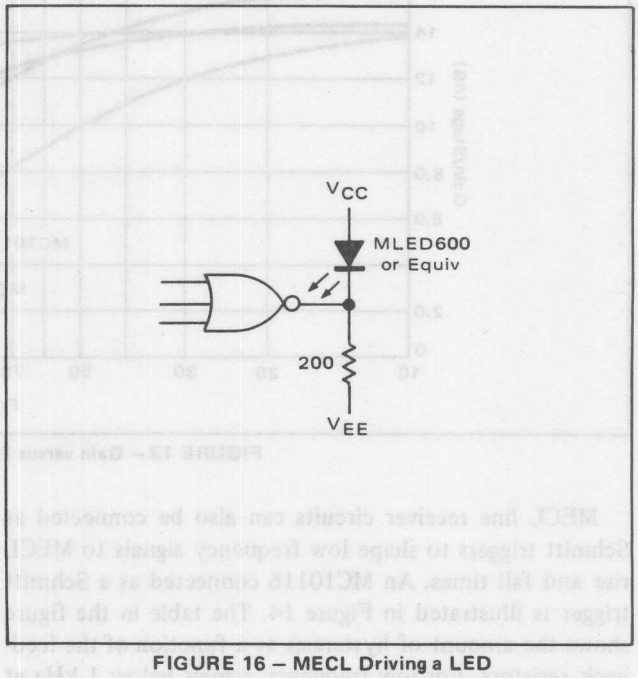

FIGURE 16 – MECL Driving a LED